



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,276	09/30/2003	Bhaskar P. Chatterjee	110350-132369	6564
25943 7590 08/23/2007 SCHWABE, WILLIAMSON & WYATT, P.C. PACWEST CENTER, SUITE 1900 1211 SW FIFTH AVENUE PORTLAND, OR 97204			EXAMINER SOFOCLEOUS, ALEXANDER	
			ART UNIT 2824	PAPER NUMBER
			MAIL DATE 08/23/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

21

Office Action Summary	Application No. 10/676,276	Applicant(s) CHATTERJEE ET AL.	
	Examiner Alexander Sofocleous	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14-18 is/are allowed.
- 6) ☒ Claim(s) 1,2,7-11,13,19,20 and 25-27 is/are rejected.
- 7) ☒ Claim(s) 3-6,12 and 21-24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>2/26/04</u> . | 6) <input checked="" type="checkbox"/> Other: <u>EAST search history</u> . |

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed September 30, 2003, and the Information Disclosure Statement filed February 26, 2004.
2. Claims 1-27 are pending in the case. Claims 1, 14, and 19 are independent claims.

Information Disclosure Statement

3. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on February 26, 2004. This IDS has been considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 1, 2, 13, 19, 20, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (U.S. Patent 6,674,671)**

Regarding claim 1, 19, and 27, Campbell et al. show a register file (see Fig. 9) comprising:

a multi-level multiplexer output circuit (see Fig. 9 [56]) coupled to a global bit trace (Fig. 9 [GBL]);

keeper circuitry (see Fig. 5 [34]) coupled to said global bit trace (see Fig. 5 [32]; see Fig. 5, 9 [Dout]).

Although Campbell et al. show a clock controlling the keeper (see Fig. 5 [CLK to 34]), Campbell et al. further teach the keeper circuit may be controlled by any other indication of the evaluate phase (see column 5, lines 28-31).

Campbell et al. are silent with respect to the specific provision of the keeper circuit connected to a driving signal, and a decoder circuit connected to the keeper to selectively decouple the driving signal from the global decoder.

However, prior art teachings of Campbell et al. show the keeper applying a driving voltage (Fig. 2 [Vdd from pmos controlled by Dout]) to the line (Fig. 2 [N1]). Further, a decoder may be used to generate signals such as "any other indication of the evaluation phase" as discussed above.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a driving voltage for the keeper and use a decoder to generate a control signal to control the keeper for the purposes of applying well-known techniques to known devices ready for improvement to yield predictable results.

The limitations directed to environment (i.e., a computer system inclusive of a processor, memory, and a bus), are well-known in the art. It is well-known in the art that computer systems, (or "systems" as recited), include at least a processor, memory, and a bus. Further, it is well-known that computer systems include a graphics processor such that a user may see output.

Therefore, it also would have been obvious to one of ordinary skill in the art at

the time of the invention to implement the above into a computer system such that the memory system discussed above may be used.

Regarding claims 2, and 20, Campbell et al. further teach the multi-level multiplexer output circuit comprises a plurality of local bit traces (see Fig. 9 [LBL0...LBLN]).

Regarding claim 13 and 26, Campbell et al. are silent with respect to the particulars of the implicit selection transistors used in multiplexer output circuit (see Fig. 9 [56]).

However, it is well-known in the art that low threshold voltage transistors have low intrinsic delays as compared to "standard" threshold voltage transistors. Such low intrinsic delay transistors would permit the increase of clock speeds in high-speed circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement low threshold voltage transistors into the mux for the purpose of permitting the circuit to operate at higher frequencies.

6. Claims 7-9, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (U.S. Patent 6,674,671) in view of AAPA (Applicant's Admitted Prior Art Fig. 1).

Regarding claims 7-9, Campbell et al. are silent with respect to local bit line precharge circuitry.

However, as exemplified in AAPA, it is well-known to include a precharge

transistor (Fig. 1 [124]) for the local bit line. Additionally, AAPA shows this precharge transistor is a PMOS transistor and a clock signal (Fig. 1 [CLK]) controls the gate of the PMOS precharge transistor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a PMOS precharge transistor for the purposes of providing well-known circuitry to the local bit lines.

Additionally, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a NMOS transistor with gate coupled to Vcc (such that the NMOS is always on, creating a connection between the PMOS and local bit line) since the addition of an NMOS provides an equivalent, or substantially equivalent, and predictable results (i.e., creating an electrical path from the PMOS to local bit line).

Regarding claim 25, Campbell et al. are silent with respect to using a upsized PMOS.

AAPA teaches an upsized PMOS (see paragraph 0008).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use an upsized PMOS for the keeper for the purposes of maintaining the precharged value on the local bit line (see paragraph 0008).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (U.S. Patent 6,674,671) in view of Levy et al. (U.S. Patent 7,034,576).

Campbell et al. are silent with respect to providing a weak keeper.

Levy et al. teach using a weak keeper (see Fig. 4 [420]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Levy et al. to Campbell et al. such that a weak keeper is used for the purposes of reducing the effective keeper strength (instead of disabling the keeper) which would counteract noise (see column 4, lines 40-44).

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (U.S. Patent 6,674,671) in view of Desai et al. (U.S. Patent 6,512,712).

Campbell et al. are silent with respect to providing a precharge transistor for the global bit line.

Desai et al. teach that it was well-known to include precharge circuitry for the global bit line (see Fig. 1 [104 to global bit line]; Fig. 2 [204 to global bit line]; Fig. 3 [304 to global bit line])

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Desai et al. to Campbell et al. such that a precharge transistor is provided for the global bit line for the purposes of including well-known precharge circuitry that yield predictable results.

Allowable Subject Matter

9. Claims 3-6, 12, and 21-24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

10. **Claims 14-18 are allowed.**

11. The following is a statement of reasons for the indication of allowable subject matter:

With respect to dependent claim 3, independent claim 14, and dependent claim 21 (and 4-6, 15-18, 22-24 which further depend), there is no teaching, suggestion, or motivation for combination in the prior art to decoupling the driving signal from the global bit line based on whether a local bit line evaluates and a corresponding select signal is asserted.

With respect to dependent claim 12, there is no teaching, suggestion, or motivation for combination in the prior art to providing a multi-level multiplexer with 3-stack pulldown.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kumar et al. (U.S. Patent 6,629,194, Hsu et al. (U.S. Patent

6,690,604), Wijeratne et al. (U.S. Patent 7,002,855), Chatterjee et al. (U.S. Patent 7,016,239), and Levy et al. (U.S. Patent 7,034,576),

Kumar et al. show a register file.

Hsu et al. show a counter applying a control signal to a keeper connected to a local bitline.

Wijeratne et al. (filed after) and Chatterjee et al. (filed same day) teach a controllable keeper connected to the local bit line.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

Art Unit: 2824

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

AGS

A handwritten signature in black ink, appearing to read 'Anh Phung', written in a cursive style.

**ANH PHUNG
PRIMARY EXAMINER**